

PROGRAMA INTERUNIVERSITARIO DE DOCTORADO



EN TECNOLOGÍAS DE LA INFORMACIÓN

MENTIÓN DE CALIDAD
PROGRAMAS DE DOCTORADO
CONVOCATORIA 2004

CONFERENCIA

“Radeon HD 2900 and Geometry Generation”



Dr. M. Doggett



Día e hora: Martes, 11 de setembro de 2007. 12:00 horas

Lugar: Sala de Xuntas do Departamento de Electrónica e Computación. USC

Resumo:

The ATI Radeon HD 2900 developed by AMD is a Graphics Processing Unit (GPU) capable of massively parallel computation for high performance 3D graphics and general purpose algorithms. The unified shader architecture consists of a combination of MIMD and SIMD architectures of 5 way scalar arithmetic units running in parallel. The shader uses multi-threading to hide latency of memory access so that compute units are keep busy. The threads consist of vertex, geometry and pixel threads that represent different programmable stages of a traditional 3D graphics pipeline mapped onto a single scheduled shader unit. Varied distributed and unified caches are used for data, instructions, read only texture reads and vertex data. A ring based memory subsystem allows multiple clients to access multiple memory channels.

The Radeon HD 2900 includes a tessellator for generating highly detailed surfaces using the GPU in a fixed function pipeline. More complex surface operations can be performed using the Direct3D10 API's new geometry shader. This shader stage allows programmable operations on the geometry in a 3D scene, not just the individual vertices or pixels. This geometry shader gives access to neighbouring vertices which allows computation of surface properties. These surface properties can then be used to generate new vertices to represent a more complex geometry then was originally sent to the GPU enabling algorithms to be run that previously needed to be run on the CPU.

